IN THE CLAIMS

1.-21. (Cancelled).

22. (Currently Amended) A Static Random Access Memory (SRAM) cell, comprising:

a first diffusion region formed on a semiconductor substrate;

a second diffusion region formed on said semiconductor substrate;

a first conductive layer formed over said semiconductor substrate;

an interlayer insulating film formed on said semiconductor substrate, said interlayer insulating film having an opening which exposes said first and second diffusion ~~layers~~ regions and said first conductive layer;

a second conductive layer formed in said opening and contacting said first and second diffusion regions;

a dielectric layer formed on said second conductive layer; and

a third conductive layer formed on said dielectric layer, whereby a capacitor is formed by said second and third conductive layers and said dielectric layer.

23. (Previously Presented) The SRAM cell as claimed in claim 22, said cell further comprising:

a first load transistor which has source and drain regions, one of which corresponds to said first diffusion region; and

a first drive transistor which has source and drain regions, one of which corresponds to said second diffusion region.

24. **(Currently Amended)** A Static Random Access Memory (SRAM) cell, comprising:

a first diffusion region formed on a semiconductor substrate;

a second diffusion region formed on said semiconductor substrate;

a first conductive layer formed over said semiconductor substrate;

an interlayer insulating film formed on said semiconductor substrate, said interlayer insulating film having an opening which exposes said first and second diffusion ~~layers~~ regions and said first conductive layer;

a second conductive layer formed in said opening;

a dielectric layer formed on said second conductive layer;

a third conductive layer formed on said dielectric layer, whereby a capacitor is formed by said second and third conductive layers and said dielectric layer;

a first load transistor which has source and drain regions, one of which corresponds to said first diffusion region;

a first drive transistor which has source and drain regions, one of which corresponds to said second diffusion region;

a second load transistor and a second drive transistor, each of said second load transistor and said second drive transistor having a gate electrode;

wherein said first conductive layer has a "T" shape having two branches, one of said branches corresponding to said second load transistor and the other of said branches corresponding to said second drive transistor.

25. **(Previously Presented)** The SRAM cell as claimed in claim 24, wherein a first contact is connected between said third conductive layer and a gate electrode of said first load transistor and of said first drive transistor, a second contact is connected between said third conductive layer and said second load transistor, and a third contact is connected between said third conductive layer and said second drive transistor.

26. **(Previously Presented)** The SRAM cell as claimed in claim 25, wherein said gate electrode, said branches and said second conductive layer are arranged in parallel with one another.

27. **(Currently Amended)** A Static Random Access Memory (SRAM) cell, comprising:

a first diffusion region formed on a semiconductor substrate;

a second diffusion region formed on said semiconductor substrate;

a first conductive layer formed over said semiconductor substrate;

an interlayer insulating film formed on said semiconductor substrate, said interlayer insulating film having an opening which exposes said first and second diffusion ~~layers~~ regions and said first conductive layer;

a second conductive layer formed in said opening;

a dielectric layer formed on said second conductive layer; and

a third conductive layer formed on said dielectric layer, whereby a capacitor is formed by said second and third conductive layers and said dielectric layer, wherein a top surface of said second conductive layer is higher than that of said interlayer insulating film.

28. **(Previously Presented)** The SRAM cell as claimed in claim 27, wherein said dielectric layer is formed on facing side surfaces of said second conductive layer.

29. **(Previously Presented)** The SRAM cell as claimed in claim 28, wherein said dielectric layer is formed on a single side of said facing side surfaces of said second conductive layer.

30. **(Previously Presented)** The SRAM cell as claimed in claim 22, wherein a top surface of said second conductive layer is lower than that of said interlayer insulating film.

31. **(Previously Presented)** The SRAM cell as claimed in claim 22, wherein said first conductive layer is formed on an element isolation layer on said semiconductor substrate.

32. **(Previously Presented)** The SRAM cell as claimed in claim 22, wherein said opening is filled with said second conductive layer.

33. **(Previously Presented)** The SRAM cell as claimed in claim 22, wherein said opening is filled with said third conductive layer.

34. **(Previously Presented)** The SRAM cell as claimed in claim 22, further comprising:

an element isolation layer formed between said first and second diffusion regions; and

a first region formed over said element isolation layer in the opening to define a space as the rest portion in the opening, wherein

said space is filled with the second conductive layer.

35. **(Previously Presented)** The SRAM cell as claimed in claim 22, further comprising:

an element isolation layer formed between said first and second diffusion regions; and

a first region formed over said element isolation layer in the opening to define a space as the rest portion in the opening, wherein

said space is filled with the third conductive layer.

36. **(Previously Presented)** The SRAM cell as claimed in claim 24, wherein

said first conductive layer has a trunk of the "T" shape, and

a bottom of said trunk directly contacts the second conductive layer.

37. **(Previously Presented)** The SRAM cell as claimed in claim 22, wherein

said second conductive layer is made of metal and

said third conductive layer is made of metal.